In the Claims:

Please add new claims 21-24. The claims are as follows:

1. (Original) A structure, comprising:

a BIST (Built-In-Self-Test) circuit; and

a first memory circuit electrically coupled to the BIST circuit,

wherein the BIST circuit is configured to perform a first test pass for the first memory circuit to collect the cycle numbers of failing cycles for the first memory circuit in response to the first memory circuit being selected for testing, and wherein, during a second test pass for the first memory circuit performed by the BIST after the first test pass for the first memory circuit, the BIST circuit is configured to collect the contents of the locations in the first memory circuit associated with the failing cycles for the first memory circuit.

2. (Original) The structure of claim 1, wherein the BIST circuit further comprises a memory circuit select register configured to receive a select value via scanning such that the first memory circuit is selected for testing.

3. (Original) The structure of claim 1, wherein the first memory circuit comprises a first data-out register configured to store a content of a location of the first memory circuit associated with a current cycle, wherein the BIST circuit comprises a BIST state register configured to store BIST control, address, and data signals of the current cycle, and wherein during a failing cycle of the second test pass for the first memory circuit, (i) the BIST circuit is configured to pause, (ii) the first data-out register and the BIST state register are electrically coupled together so as to form a

first diagnostic shifting loop, and (iii) the contents of the first data-out register and the BIST state register are shifted in the first diagnostic shifting loop such that the contents of the first data-out register and the BIST state register can be extracted out of the structure, and such that, after the shift, the first data-out register and the BIST state register have the same contents as before the shift.

4. (Original) The structure of claim 3, wherein the BIST circuit further comprises a BIST multiplexer configured to electrically couple the first data-out register and the BIST state register together so as to form the first diagnostic shifting loop during a failing cycle of the second test pass for the first memory circuit and in response to the first memory circuit being selected for testing.

5. (Original) The structure of claim 3, further comprising a chip multiplexer configured to electrically couple the first data-out register to a tester during a failing cycle of the second test pass for the first memory circuit and in response to the first memory circuit being selected for testing, wherein the contents of the first data-out register and the BIST state register are extracted to the tester via the chip multiplexer in response to the contents of the first data-out register and the BIST state register being shifted in the first diagnostic shifting loop.

6. (Original) The structure of claim 5, wherein the first memory circuit further comprises:

a first comparator electrically coupled to the first data-out register and the BIST circuit; and

a first mode multiplexer electrically coupled to the first comparator and the first data-out register,

wherein in response to the BIST circuit executing a cycle which is not a failing cycle of the second testing pass for the first memory circuit, the first mode multiplexer is configured to electrically couple the first comparator to the chip multiplexer, and wherein in response to the BIST circuit executing a failing cycle of the second testing pass for the first memory circuit, the first mode multiplexer is configured to electrically couple the first data-out register to the chip multiplexer.

7. (Original) The structure of claim 3, further comprising a second memory circuit electrically coupled to the BIST circuit, wherein the BIST circuit is configured to perform a first test pass for the second memory circuit to collect the cycle numbers of failing cycles for the second memory circuit in response to the second memory circuit being selected for testing, and wherein, during a second test pass for the second memory circuit performed by the BIST after the first test pass for the second memory circuit, the BIST circuit is configured to collect the contents of the locations of the second memory circuit associated with the failing cycles for the second memory circuit.

8. (Original) The structure of claim 7, wherein the second memory circuit comprises a second data-out register configured to store a content of a location of the second memory circuit associated with a current cycle, and wherein during a failing cycle of the second test pass for the second memory circuit, (i) the BIST circuit is configured to pause, (ii) the second data-out register and the BIST state register are electrically coupled together so as to form a second

diagnostic shifting loop, and (iii) the contents of the second data-out register and the BIST state register are shifted in the second diagnostic shifting loop such that the contents of the second data-out register and the BIST state register can be extracted out of the structure, and such that the second data-out register and the BIST state register have the same contents as before the shift.

9. (Original) A method for testing a structure, the method comprising the steps of:

providing in the structure a BIST (Built-In-Self-Test) circuit and a first memory circuit electrically coupled to the BIST circuit;

using the BIST circuit to perform a first test pass for the first memory circuit to collect the cycle numbers of failing cycles for the first memory circuit in response to the first memory circuit being selected for testing; and

after performing the first test pass for the first memory circuit, using the BIST circuit to perform a second test pass for the first memory circuit to collect the contents of the locations in the first memory circuit associated with the failing cycles for the first memory circuit.

10. (Original) The method of claim 9, further comprising the step of using a memory circuit select register to receive a select value via scanning so as to select the first memory circuit for testing.

11. (Original) The method of claim 9, further comprising steps of:

providing in the first memory circuit a first data-out register configured to store a content of a location of the first memory circuit associated with a current cycle;

providing in the BIST circuit a BIST state register configured to store BIST control, address, and data signals of the current cycle; and

during a failing cycle of the second test pass for the first memory circuit, (i) pausing the BIST circuit, (ii) electrically coupling the first data-out register and the BIST state register together so as to form a first diagnostic shifting loop, (iii) shifting the contents of the first data-out register and the BIST state register in the first diagnostic shifting loop such that the first data-out register and the BIST state register have the same contents as before the shift, and (iv) extracting the contents of the first data-out register and the BIST state register from the first diagnostic shifting loop out of the structure during the shift.

12. (Original) The method of claim 11, further comprising the step of using a BIST multiplexer in the BIST circuit to electrically couple the first data-out register and the BIST state register together so as to form the first diagnostic shifting loop during a failing cycle of the second test pass for the first memory circuit and in response to the first memory circuit being selected for testing.

13. (Original) The method of claim 11, further comprising the steps of:

using a chip multiplexer to electrically couple the first data-out register to a tester during a failing cycle of the second test pass for the first memory circuit and in response to the first memory circuit being selected for testing; and

extracting the contents of the first data-out register and the BIST state register to the tester via the chip multiplexer in response to the contents of the first data-out register and the BIST

state register being shifted in the first diagnostic shifting loop.

14. (Original) The method of claim 13, further comprising the steps of:

providing a first comparator electrically coupled to the first data-out register and the BIST circuit;

providing a first mode multiplexer electrically coupled to the first comparator and the first data-out register;

using the first mode multiplexer to electrically couple the first comparator to the chip multiplexer in response to the BIST circuit executing a cycle which is not a failing cycle of the second testing pass for the first memory circuit; and

using the first mode multiplexer to electrically couple the first data-out register to the chip multiplexer in response to the BIST circuit executing a failing cycle of the second testing pass for the first memory circuit.

15. (Original) The method of claim 11, further comprising the steps of:

providing in the structure a second memory circuit electrically coupled to the BIST circuit;

using the BIST circuit to perform a first test pass for the second memory circuit to collect the cycle numbers of failing cycles for the second memory circuit in response to the second memory circuit being selected for testing; and

after performing the first test pass for the second memory circuit, using the BIST circuit to perform a second test pass for the second memory circuit to collect the contents of the

locations in the second memory circuit associated with the failing cycles for the second memory circuit.

16. (Original) The method of claim 15, further comprising the steps of:

providing in the second memory circuit a second data-out register configured to store a content of a location of the second memory circuit associated with a current cycle; and

during a failing cycle of the second test pass for the second memory circuit, (i) pausing the BIST circuit, (ii) electrically coupling the second data-out register and the BIST state register together so as to form a second diagnostic shifting loop, (iii) shifting the contents of the second data-out register and the BIST state register in the second diagnostic shifting loop such that the second data-out register and the BIST state register have the same contents as before the shift, and (iv) extracting the contents of the second data-out register and the BIST state register from the second diagnostic shifting loop out of the structure during the shift.

17. A method for testing a memory chip, the method comprising the steps of:

providing in the memory chip a RAM (Random Access Memory) and a BIST (Built-In-Self-Test) circuit;

providing a RAM select register in the BIST circuit;

scanning in a select value into the RAM select register so as to select the RAM for testing;

using the BIST circuit to test the RAM for a first test pass to collect the cycle numbers of failing cycles in response to the RAM being selected for testing; and

after testing the RAM for the first test pass, using the BIST circuit to test the RAM for a second test pass, wherein the second test pass comprises the same sequence of cycles as the first test pass, and wherein during the second test pass, the BIST circuit pauses at each failing cycle so that the contents of the locations of the RAM associated with the failing cycles can be extracted out of the memory chip.

18. (Original) The method of claim 17, wherein the step of using the BIST circuit to test the RAM for the first test pass to collect the cycle numbers of the failing cycles in response to the RAM being selected for testing comprises the steps of, for each cycle of the first test pass:

using a data-out register in the RAM to store the content of a location in the RAM associated with the cycle;

using a comparator in the RAM to compare the content of the data-out register and an expected value from the BIST circuit and to generate a fail signal if the content of the data-out register and the expected value are not equal;

using a mode multiplexer to pass the fail signal from the comparator to a chip multiplexer; and

using the chip multiplexer to pass the fail signal from the mode multiplexer to a tester outside the memory chip.

19. (Original) The method of claim 18, wherein the step of using the BIST circuit to test the RAM for the second test pass comprises the steps of, during each failing cycle:

pausing the BIST circuit;

forming a diagnostic shifting loop comprising a BIST state register in the BIST circuit, the data-out register, the mode multiplexer, and the RAM select register, wherein the BIST state register stores the BIST control, address, and data signals associated with the current failing cycle;

shifting the contents of the BIST state register and the data-out register in the diagnostic shifting loop; and

extracting the contents of the BIST state register and the data-out register from the diagnostic shifting loop to the tester via the BIST multiplexer and chip multiplexer.

20. (Original) The method of claim 19, wherein the step of forming the diagnostic shifting loop comprises the steps of:

using the tester to generate a diagnostic shifting signal to the BIST state register and the data-out register so as to switch them to shift registers; and

using the mode multiplexer to electrically couple the data-out register to the BIST state register in response to the diagnostic shifting signal being generated; and

using the tester to generate a diagnostic shifting signal to the BIST finite state machine so as to cause the finite state machine to be temporarily paused so that it holds it's current state, while shifting the data in the diagnostics shifting loop.

21. (New) The structure of claim 1, wherein the first test pass comprises a plurality of cycles such that each cycle of the plurality of cycles is selected from the group consisting of a read cycle, a

write cycle, and a setup cycle, wherein the setup cycle is within the BIST and does not include reading from or writing to any random access memory (RAM), and wherein the second test pass comprises said plurality of cycles.

22. (New) The structure of claim 21, wherein a first cycle of the plurality of cycles includes the setup cycle.

23. (New) The method of claim 9, wherein the first test pass comprises a plurality of cycles such that each cycle of the plurality of cycles is selected from the group consisting of a read cycle, a write cycle, and a setup cycle, wherein the setup cycle is within the BIST and does not include reading from or writing to any random access memory (RAM), and wherein the second test pass comprises said plurality of cycles.

24. (New) The method of claim 23, wherein a first cycle of the plurality of cycles includes the setup cycle.